PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10078732	02/19/2002	716	8	2825	Tat

**APPLICANTS: Tseng Kenneth;

**CONTINUING DATA VERIFIED: BT

** FOREIGN APPLICATIONS VERIFIED: BT

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☑ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☑ no		07716P001
Verified and Acknowledged Examiner's initials	BT		

TITLE : Variable stage ratio buffer insertion for noise optimization in a logic network

U.S DEPT. OF COMM./PAT.& TM-PTO-436L(Rev 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid		DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	Primary Examiner PREPARED FOR ISSUE	Application Examiner

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